WEST Search History

DATE: Friday, May 02, 2003

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L7	L6 and l3	38	L7
L6	@ay<=1997	15940797	L6
L5	(phase near2 lock$3 near2 loop$3) same (charge near pump$3) same (current near2 switch$3) same (electrod$)	0	L5
L4	(phase near2 lock$3 near2 loop$3) same(charge near pump$3) same (current near2 switch$3) same (electrod$)	0	L4
L3	(phase near2 lock$3 near2 loop$3) and (charge near pump$3) and (current near2 switch$3) and (electrod$)	67	L3
L2	(phase near2 lock$3 near2 loop$3) and (charg near pump) and (current near2 switch$3) and (electrod$)	0	L2
L1	(phase near2 lock$3 near2 loop$3) same (charg near pump) same (current near2 switch$3) same (electrod$)	0	L1

END OF SEARCH HISTORY

L7: Entry 14 of 38 File: USPT Nov 8, 1994

DOCUMENT-IDENTIFIER: US 5362990 A
TITLE: Charge pump with a programmable pump current and system

Abstract Text (1):
A charge pump has a reference circuitry (18, 20, 22), a first parallel current path (16), at least one second parallel current path (16), a mirror circuit (46), a sourcing circuitry (60, 62) and a sinking circuitry (50, 54, 66, 68). The first and the at least one second parallel current path sink current from a first node responsive to a predetermined voltage generated by the reference circuitry. The at least one second current path also operates responsive to a control signal. The mirror circuit generates a second predetermined voltage responsive to the total current sunk from the first node. The sourcing circuitry and the sinking circuitry sourcing and sinking a current from the output node, respectively, responsive to the second predetermined voltage and to a control signal. The disclosed charge pump may be incorporated into a phase locked loop circuit where constant stability parameters are desired.

Application Filing Year (1):
1993

Brief Summary Text (2):
The present invention generally relates to charge pumps, and more specifically to a charge pump with a programmable pump current.

Brief Summary Text (4):
Charge pumps are a class of circuits that deliver a known current to a node. Charge pumps are frequently used in phase locked loop circuits (hereafter simply PLLs). A PLL matches the phase and frequency of a self-generated clock signal to a reference clock signal. In a PLL, a charge pump sinks current, sources current or is in a high impedance state with respect to an output node responsive to the phase and frequency differences between the self-generated clock signal and the reference clock signal. A resistor and a capacitor are connected in series (an RC circuit) between the output node and ground. The output node is also connected to a gate of a transistor. By selectively sinking or sourcing current to the output node, the gate to source voltage of the transistor, and thus, the conductivity of the transistor may be adjusted. Typically, the transistor connects a voltage supply rail to the various sources of one or more inverters. The inverters are connected in series forming a ring oscillator. By adjusting the charge at the output node, the charge pump can adjust the propagation delay of a signal through the ring oscillator and, hence, the frequency of the self-generated clock signal.

Brief Summary Text (6):
The frequency of a PLL's self-generated clock signal may be programmed dynamically by inserting a programmable divider in its path. A PLL incorporating such a divider may generate a clock signal with different frequencies depending upon the settings of the inserted divider circuit. The PLL has a set of stability parameters associated with it for each different divider setting. Generally, it is desirable to have each of these sets of parameters as close to every other set as possible. One method of maintaining a constant set of stability parameters is to vary the current that the charge pump sources or sinks to the output node and to the RC circuit. As described above, the voltage at the output node controls the frequency of the voltage controlled oscillator.

Brief Summary Text (7):
Known programmable current charge pumps have certain disadvantages associated with

them. In general, they are slower, larger, require more power and have greater output capacitance than non-programmable charge pumps. Their use, to now, has been a compromise.

Brief Summary Text (9):
In accordance with the present invention, there is disclosed a charge pump having a programmable output current which substantially eliminates disadvantages of prior charge pumps.

Brief Summary Text (10):
A charge pump has a reference circuitry, a first parallel current path, at least one second parallel current path, a mirror circuit, a sourcing circuitry and a sinking circuitry. The first and the at least one second parallel current paths sink current from a first node responsive to a predetermined voltage generated by the reference circuitry. The at least one second current path also operates responsive to a control signal. The mirror circuit generates a second predetermined voltage responsive to the total current sunk from the first node. The sourcing circuitry and the sinking circuitry sourcing and sinking a current from the output node, respectively, responsive to the second predetermined voltage and to a control signal.

Drawing Description Text (3):
FIG. 1 depicts a partial schematic diagram of a programmable charge pump constructed in accordance with the present invention; and

Drawing Description Text (4):
FIG. 2 depicts a block diagram of a phase locked loop incorporating the programmable charge pump depicted in FIG. 1.

Detailed Description Text (2):
FIG. 1 depicts a partial schematic diagram of a programmable charge pump (hereafter simply pump) 10 constructed in accordance with the present invention. Pump 10 is operable to source or sink a known amount of current to an output node 12 for a given period of time. Pump 10 thereby dynamically controls the voltage present at output node 12 (labeled V.sub.OUT). The current that pump 10 sources or sinks to output node 12 is programmable by a set of N logic signals 14 (labeled CONTROL-A, CONTROL-B, etc.) where N is a integer. Pump 10 has a plurality of parallel current paths 16. The amount of current that pump 10 sources or sinks is determined by the number and individual sizes of the enabled ones of these parallel current paths 16. Each one of the logic signals 14 enables or disables a selected differing one of the parallel current paths 16.

Detailed Description Text (3):
The amount of current that pump 10 sources or sinks to output node 12 may be advantageously used to maintain certain stability characteristics of a circuit incorporating pump 10 over a range of operating modes. These stability characteristics include the damping coefficient and natural frequency of a circuit incorporating pump 10. The location of parallel current paths 16 away from output node 12 allows pump 10 to turn on and off more quickly than known charge pumps. Also, the same set of parallel current paths is used to both source and sink current to output node 12. Prior charge pumps use two sets of parallel current paths: one set for sourcing current to an output node and one set for sinking current from the output node. The disclosed invention allows a charge pump to be designed with fewer transistors thus decreasing the pump's size.

Detailed Description Text (4):
Continuing with FIG. 1, a reference current generator 18 generates a reference current, I.sub.REF. A first terminal of reference current generator 18 is connected to a drain and to a gate of a P-channel transistor 20. A second terminal of reference current generator 18 is connected to a terminal of a first voltage supply (labeled GND).The gate of transistor 20 is connected to a gate of a P-channel transistor 22. A source of transistor 20 is connected to a drain of a P-channel transistor 24. A gate and a source of transistor 24 are connected to a logic signal CHARGE-PUMP-ENABLE and to a terminal of a second voltage supply (labeled V.sub.DD), respectively. A drain of transistor 22 is connected to a source of an N-channel

transistor 26. A drain of transistor 26 is connected to a terminal of the first voltage supply. A gate of transistor 26 is connected to the source of transistor 26.

Detailed Description Text (5):
Each of the N parallel current paths 16 is connected in parallel between a first node 28 and a second node 30. The second node is connected to a terminal of the second voltage supply. Each current path has a switch and a transistor. The switch places the current path in a either a high impedance state or a conducting state. The transistor in each current path causes a known current to flow through the current path depending upon the transistor biasing. In the depicted embodiment, pump 10 has two such parallel paths and a third, modified current path. The third modified current path is always operating. It provides a minimum current output when pump 10 is operating.

Detailed Description Text (6):
The first current path has a switch or pass gate 32 and an N-channel transistor 34 connected in series. A first terminal of pass gate 32 is connected to first node 28. A second terminal of pass gate 32 is connected to a drain of transistor 34. A gate of transistor 34 is connected to the gate of transistor 26. A source of transistor 34 is connected to node 30. A P-channel device and an N-channel device of pass gate 32 are connected to an output of an inverter 36 and to the logic signal CONTROL-A, respectively. An input of inverter 36 is connected to the logic signal CONTROL-A.

Detailed Description Text (7):
The second current path has a switch or pass gate 38 and an N-channel transistor 40 connected in series. A first terminal of pass gate 38 is connected to first node 28. A second terminal of pass gate 38 is connected to a drain of transistor 40. A gate of transistor 40 is connected to the gate of transistor 26. A source of transistor 40 is connected to node 30. A P-channel device and an N-channel device of pass gate 32 are connected to an output of an inverter 42 and to the logic signal CONTROL-B, respectively. An input of inverter 36 is connected to the logic signal CONTROL-B.

Detailed Description Text (10):
First node 28 is connected to a drain and a gate of a P-channel transistor 46. A source of transistor 46 is connected to a drain of a P-channel transistor 48. A gate and a source of transistor 48 are connected to the logic signal CHARGE-PUMP-ENABLE and to a terminal of the second voltage supply, respectively. The gates of transistor 46 and 48 are connected to a gate of P-channel transistor 50 and to a gate of a P-channel transistor 52, respectively. A source of transistor 52 is connected to a terminal of the second voltage supply. A drain of transistor 52 is connected to a source of transistor 50. A drain of transistor 50 is connected to a drain and a gate of an N-channel transistor 54. A source of transistor 54 is connected to a drain of an N-channel transistor 56. A gate and a source of transistor 56 are connected to an output of an inverter 58 and to a terminal of the second voltage supply, respectively. An input of inverter 58 is connected to the logic signal CHARGE-PUMP-ENABLE.

Detailed Description Text (12):
Charge pump 10 operates when the signal CHARGE-PUMP-ENABLE is asserted. Consistent with standard nomenclature, a superscript bar indicates an active low logic signal. When the signal CHARGE-PUMP-ENABLE is asserted, transistors 48, 24 and 52 are placed in a conducting state. Therefore, transistors 46, 22, 20 and 50 are connected to the second voltage supply. In addition, the signal CHARGE-PUMP-ENABLE, inverted by inverter 58, places transistor 56 into a conducting state. Therefore, transistor 54 is connected to the first voltage supply. Charge pump 10 does not consume any power when the signal CHARGE-PUMP-ENABLE is not asserted. This feature is useful in at least two instances. First, this feature may be integrated into a power management scheme of a data processor incorporating charge pump 10. Second, the non-assertion of the signal CHARGE-PUMP-ENABLE may be used to detect any electrical short-circuits with charge pump 10. These short-circuits will consume power even when the signal CHARGE-PUMP-ENABLE is not asserted.

Detailed Description Text (13):
When the signal CHARGE-PUMP-ENABLE is asserted, charge pump 10 has three modes of

operation: charge output node 12, discharge output node 12 and place output node 12 into a high impedance state. In each of these three modes of operation, transistor 46 mirrors a programmed voltage level to transistor 60 and 66. The generation of this programmed voltage level is described below. The voltage level present on the gate of transistor 46 causes a current to flow through transistor 60, through transistor 66, or through neither transistor.

Detailed Description Text (14):
The logic signals PUMP-UP and PUMP-DOWN determine in which of the three modes charge pump 10 operates. If the signal PUMP-UP is asserted and the signal PUMP-DOWN is not asserted, then transistor 62 will be in a conducting state and transistor 68 will be in a non-conducting state. Therefore, transistor 60 will source an amount of current to output node 12 determined by the voltage level present on the gate of transistor 46. If the signal PUMP-UP is not asserted and the signal PUMP-DOWN is asserted, then transistor 62 will be in a non-conducting state and transistor 68 will be in a conducting state. Therefore, transistor 66 will sink an amount of current from output node 12 determined by the voltage level present on the gate of transistor 46. If neither of the two signals is asserted, then both transistors 62 and 68 will be in a non-conducting state. Therefore, output node 12 is placed into a high impedance state. (The assertion of both PUMP-UP and PUMP-DOWN is an illegal state.)

Detailed Description Text (17):
The previous description assumes that the individual transistors depicted in FIG. 1 are identical. Identical transistors generate identical currents when biased with the same gate-source voltage differential. Embodiments of the disclosed invention with different assumptions are possible. For instance, each of the transistors within the parallel current paths 16 may be sized differently to generate a wider range of sum currents at node 28. As is known in the art, the size of a transistor relates to the dimensions of a transistor's gate. The ratio of gate sizes of three transistors in three parallel current paths each to transistor 26 might be one, two, and four. This ratio would allow the sum current at node 28 to vary from I.sub.REF to (7*I.sub.REF) in increments of I.sub.REF depending upon the particular inputs to the three logic signals, CONTROL-A, CONTROL-B and CONTROL-C. Other transistor modifications may advantageously increase or decrease the effective output of reference current generator 18. The set of all possible output currents may be linearly scaled by increasing or decreasing the ratio of the sizes of certain other transistors. For instance, the size of transistor 26 may be halved with respect to transistors 34, 40, etc. This modification will double the current that flows through transistors 34, 40, etc. with respect to transistor 26. A charge pump with such a modification doubles the current sourced or sunk at output node 12 relative to a charge pump without the modification.

Detailed Description Text (18):
Transistors 52 and 56, respectively, ensure that transistors 60 and 66 are biased correctly. As described above, transistor 60 mirrors the current flowing through transistor 50 by having the same gate-source voltage differential. Similarly, transistor 66 mirrors the current flowing through transistors 54 by having the same gate-source voltage differential. However, the sources of both transistors 60 and 66 are not directly connected to a voltage supply terminal. In particular, transistor 60 is connected to the second voltage supply through transistor 62. Transistor 66 is connected to the first voltage supply through transistor 68. These connections, or their equivalent, are necessary to the operation of charge pump 10. Therefore, transistor 52 is connected between transistor 50 and the second voltage supply, and transistor 56 is connected between transistor 54 and the first voltage supply. The resulting circuit symmetry ensures that appropriate pairs of gate-source voltage differentials are identical.

Detailed Description Text (19):
The separation of node 28 from output node 12 has several advantages. First, the output of charge pump 10 is more responsive to changes in the logic signals PUMP-UP and PUMP-DOWN. The gate-source voltage of transistor 46 constantly biases transistors 60 and 66 when enabled by the logic signal CHARGE-PUMP-ENABLE. Prior charge pumps bias the parallel current paths with the "pump-up" and "pump-down" logic signals. This approach requires additional time for the output node to begin sinking or sourcing current as each current mirror stage turns on. Second, the

number of parallel current paths is halved. Charge pump 10 has a single set of parallel current paths that sink a programmable amount of current from node 28. However, parallel current paths 16 are connected to transistors 60 and 66 in such a way as to allow charge pump 10 to sink current from or source current to output node 12. Known programmable charge pumps require a first set of parallel current paths to sink current from an output node and a second set of parallel current paths to source current to the output node. The elimination of one set of parallel current paths results in a smaller charge pump 10. Third, the capacitance of the sources of transistors 60 and 66 is determined primarily by the widths of the drains of these transistors. The capacitance of prior charge pumps is determined by each of the drains in two sets of parallel current path transistors connected to the output node. Therefore, the disclosed charge pump has a smaller output capacitance. This reduction in capacitance allows charge pump 10 to charge/discharge the output node quicker or allows for a smaller reference current generator given the same performance criteria. Fourth, charge pump 10 may operate with a voltage differential of only 3.3 volts between power rails (V.sub.DD and GND). Known programmable charge pumps have been designed to be powered by a greater voltage differential.

Detailed Description Text (20):
FIG. 2 depicts a block diagram of a phase locked loop 72 incorporating programmable charge pump 10 depicted in FIG. 1. PLL 72 has a phase/frequency detector 74, charge pump 10, a voltage controlled oscillator (hereafter simply "VCO") 76, and a divide-by-N circuit 78.

Detailed Description Text (22):
As described above in connection with FIG. 1, charge pump 10 charges or discharges output node 12 responsive to the output signals UP and DOWN of PLL 74. As depicted, the outputs UP and DOWN are connected to the charge pump inputs PUMP-UP and PUMP-DOWN, respectively. The input CHARGE-PUMP-ENABLE of charge pump 10 is connected to the signal labeled CHARGE-PUMP-ENABLE. The inputs CONTROL-A, CONTROL-B, etc. of charge pump 10 are each connected to one of the signals within the group of signals labeled FREQUENCY CONTROL.

Detailed Description Text (23):
VCO 76 generates a periodic clock signal at its output, OUT, responsive to the analog voltage at its input, IN. The input IN is connected to output node 12 of charge pump 10. As described above, VCO 76 may have within it a ring oscillator. Generally, an increase in the voltage present on output node 12 causes the frequency of the output clock signal to increase. Conversely, a decrease in the voltage present on output node 12 causes the frequency of the output clock signal to decrease. Other embodiments may reverse the relationship between frequency and output node voltage.

Detailed Description Text (26):
PLL 72 may be characterized by at least two stability parameters: a damping coefficient, D, and a natural frequency, w. These parameters are functions of the integer N and of the output current of charge pump 10, I: ##EQU1## As described above, it is desirable to maintain these parameters across as wide a range of configurations as possible. The output current of charge pump 10 may be programmed so that the ratio (I/N) is constant by enabling more or less of the parallel current paths depicted in FIG. 1. For instance, if the FREQUENCY CONTROL signals are selected so that N doubles from a first to a second time (the frequency of OUTPUT CLOCK SIGNAL doubles), then I may be doubled by enabling an additional number of parallel current paths. Consequently, the two stability parameters, D and w, will remain the same from the first to the second time.

Detailed Description Text (27):
Although the present invention has been described with reference to a specific embodiment, further modifications and improvements will occur to those skilled in the art. For instance, the designation of an electrode of a transistor as a source or drain is dependent upon the media in which a particular embodiment is made and upon the voltage supply connections. The disclosed invention may be implemented in media other than complementary metal oxide silicon (CMOS), such as bipolar and BiCMOS. Therefore, the terms source, drain and gate will be replaced with first current electrode, second current electrode and control electrode. It is to be

understood therefore, that the invention encompasses all such modifications that do not depart from the spirit and scope of the invention as defined in the appended claims.

CLAIMS:

1. A charge pump comprising:

reference circuitry for generating a first predetermined voltage;

a first parallel current path coupled to a first node the first parallel current path being operable to sink a first current from the first node in response to the first predetermined voltage;

at least one second parallel current path coupled to the first node, each of the at least one second current path being operable to sink a current from the first node in response to the first predetermined voltage and to a first selected control signal of a plurality of control signals,

a mirror circuit coupled to the first node, the mirror circuit operable to generate a second predetermined voltage responsive to a total current sunk from the first node, wherein the mirror circuit comprises a first transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode and the control electrode coupled to the first node;

sourcing circuitry coupled to an output node and to the mirror circuit for sourcing a current to the output node in response to the second predetermined voltage and to a second selected control signal of the plurality of control signals, and

sinking circuitry coupled to the output node and to the mirror circuit for sinking a current from the output node in response to the second predetermined voltage and to a third selected control signal of the plurality of control signals.

2. The charge pump of claim 1 wherein the sourcing circuitry comprises:

a second transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to a terminal of a first voltage supply, the control electrode coupled to the second selected control signal of the plurality of control signals; and

a third transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the second current electrode of the second transistor, the second current electrode coupled to the output node, the control electrode coupled to the control electrode of the first transistor.

3. The charge pump of claim 2 wherein the sinking circuitry comprises:

a fourth transistor comprising a first current electrode, a second current electrode and a control electrode, the control electrode coupled to the control electrode of the first transistor; and

a fifth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode and the control electrode coupled to the first current electrode of the fourth transistor;

a sixth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the output node, the control electrode coupled to the control electrode of the fifth transistor; and

a seventh transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the second current electrode of the sixth transistor, the second current electrode coupled to a terminal of a second voltage supply, the control electrode coupled to the third selected control signal of the plurality of control signals.

4. The charge pump of claim 3 wherein the sinking circuitry further comprises an eighth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the second current electrode of the fifth transistor, the second current electrode coupled to a terminal of the second voltage supply, the control electrode coupled to a selected control signal of the plurality of control signals.

5. A charge pump comprising:

reference circuitry for generating a predetermined voltage;

a first node;

a second node for receiving a first voltage supply;

at least one parallel current path, each of the at least one parallel current path comprising:

a first transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the second node, the control electrode coupled to the predetermined voltage; and

a switch means comprising first and second terminals, the first terminal of the switch means coupled to the first node, the second terminal coupled to the second current electrode of the first transistor, the switch means being in a conductive state in response to a first logic state of a first selected control signal of a plurality of control signals and being in a high impedance state in response to a second logic state of the first selected control signal;

a second transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode and the control electrode coupled to the first node, the second current electrode receiving a second voltage supply;

an output node;

sourcing circuitry coupled to the output node and to the second node for sourcing a predetermined current to the output node in response to a voltage present at the control electrode of the second transistor and a second selected control signal of the plurality of control signals; and

sinking circuitry coupled to the output node and to the second node for sinking the predetermined current to the output node in response to the voltage present at the control electrode of the second transistor and to a selected control signal of the at least one control signal.

6. The charge pump of claim 5 wherein the sourcing circuitry comprises:

a third transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to a terminal of the second voltage supply, the control electrode coupled to the second selected control signal of the plurality of control signals; and

a fourth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the second current electrode of the third transistor, the second current electrode coupled to the output node, the control electrode coupled to the control electrode of the second transistor.

7. The charge pump of claim 6 wherein the sinking circuitry comprises:

a fifth transistor comprising a first current electrode, a second current electrode and a control electrode, the control electrode coupled to the control electrode of the second transistor;

a sixth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode and the control electrode coupled to the first current electrode of the fifth transistor;

a seventh transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the output node, the control electrode coupled to the control electrode of the sixth transistor; and

an eighth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the second current electrode of the seventh transistor, the second current electrode coupled to a terminal of the first voltage supply, the control electrode coupled to the third selected control signal of the plurality of control signals.

8. The charge pump of claim 7 wherein the sinking circuitry further comprises a ninth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to the second current electrode of the sixth transistor, the second current electrode coupled to a terminal of the first voltage supply, the control electrode coupled to a selected control signal of the plurality of control signals.

9. The charge pump of claim 8 wherein the reference circuitry comprises:

a current generator having a first and a second terminal, the current generator causing a predetermined electrical current to flow from the first terminal to the second terminal, the second terminal coupled to a terminal of the first voltage supply;

a tenth transistor comprising a first current electrode, a second current electrode and a control electrode;

an eleventh transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode and the control electrode coupled to the control electrode of the tenth transistor, the first current electrode also coupled to the first terminal of the current generator; and

a twelfth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode and the control electrode coupled to the first current electrode of the tenth transistor, the second current electrode coupled to a terminal of the first voltage supply, the control electrode generating the predetermined voltage.

10. The charge pump of claim 9 further comprising:

a thirteenth transistor comprising a first current electrode a second current electrode and a control electrode, the first current electrode coupled to a terminal of the second voltage supply, the second current electrode coupled to the second current electrode of the second transistor, the control electrode coupled to another selected control signal of the plurality of control signals;

a fourteenth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to a terminal of the second voltage supply, the second current electrode coupled to the second current electrode of the fifth transistor, the control electrode coupled to said another selected control signal of the plurality of control signals; and

a fifteenth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to a terminal of the second voltage supply, the second current electrode coupled to the second current electrodes of the tenth and eleventh transistors, the control electrode coupled to said another selected control signal of the plurality of control signals.

11. The charge pump of claim 8 further comprising:

a tenth transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to a terminal of the second voltage supply, the second current electrode coupled to the second current electrode of the second transistor, the control electrode coupled to another selected control signal of the plurality of control signals; and

a eleventh transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode coupled to a terminal of the second voltage supply, the second current electrode coupled to the second current electrode of the fifth transistor, the control electrode coupled to said another selected control signal of the plurality of control signals.

12. A system comprising:

a detector for receiving a first clock signal and a second clock signal, the detector being operable to generate a subset of a plurality of control signals in response to a predetermined phase and frequency relationship of the first and second clock signals;

a charge pump coupled to the plurality of control signals, the charge pump comprising:

reference circuitry for generating a first predetermined voltage;

a first parallel current path coupled to a first node, the first parallel current path being operable to sink a first current from the first node in response to the first predetermined voltage;

at least one second parallel current path coupled to the first node, each of the at least one second current path being operable to sink a current from the first node in response to the first predetermined voltage and to a first selected control signal of the plurality of control signals;

a mirror circuit coupled to the first node, the mirror circuit operable to generate a second predetermined voltage responsive to a total current sunk from the first node, wherein the mirror circuit comprises a first transistor comprising a first current electrode, a second current electrode and a control electrode, the first current electrode and the control electrode coupled to the first node;

sourcing circuitry coupled to an output node and to the mirror circuit for sourcing a current to the output node responsive to the second predetermined voltage and to a second selected control signal of the plurality of control signals; and

sinking circuitry coupled to the output node and to the mirror circuit for sinking a current from the output node in response to the second predetermined voltage and to a third selected control signal of the plurality of control signals; and

a voltage controlled oscillator coupled to the output node of the charge pump, the voltage controlled oscillator operable to generate a third clock signal, the third clock signal characterized by a first frequency, the first frequency responsive to a voltage at the output node of the charge pump.

13. The charge pump of claim 12 further comprising a divide-by-N circuit for receiving the third clock signal, the divide-by-N circuit being operable to generate the second clock signal the second clock signal characterized by a second frequency, the ratio of the second and first frequencies is responsive to one of the plurality of control signals.

L7: Entry 4 of 38 File: USPT Aug 10, 1999

DOCUMENT-IDENTIFIER: US 5936445 A
TITLE: PLL-based differential tuner circuit

Application Filing Year (1):
1997

Brief Summary Text (8):
Another consideration in designing higher frequency continuous-time filters is variations in filter frequency response caused by variations in fabrication process, temperature and power supply. To compensate for these variations, tuner circuits have been developed that are used along with the filter to tune its frequency response. FIG. 2 shows a conventional tuner circuit. The tuner circuit includes a sine-wave voltage-controlled oscillator (VCO) 100 whose outputs connect to inputs of a comparator 102. A phase detector 104 compares the phases between an external reference square-wave CLKA and the square-wave equivalent of the output of VCO 100, CLKB. Phase detector 104 generates at its output digital UP and DN pulses for a current output charge pump 106. Charge pump 106 provides the control voltage V.sub.C to VCO 100, through its R and C loop filter components.

Brief Summary Text (15):
In yet another embodiment, the present invention provides a tuner circuit for use with continuous-time RMC filters, the tuner circuit includes a voltage-controlled oscillator a differential pair of output terminals, a comparator having a differential pair of input terminals coupled to the differential pair of output terminals of the voltage-controlled oscillator, a phase detector having a first input terminal coupled to an output of the comparator and a second input terminal coupled to an external clock signal, and a differential charge pump circuit receiving first and second control signals from the phase detector, and supplying a differential pair of voltage signals to the voltage-controlled oscillator. The charge pump circuit includes an operational amplifier having a differential pair of input terminals and a differential pair of output terminals, a first pair of current source devices coupled to a first terminal of the differential pair of input terminals of the operational amplifier, and a second pair of current source devices coupled to a second terminal of the differential pair of input terminals of the operational amplifier, wherein the first and second pair of current source devices are controlled by the first and second control signals from the charge pump circuit.

Drawing Description Text (9):
FIG. 7B shows an exemplary implementation of a differential switched current source circuit for use in the charge pump circuit of the tuner of FIG. 7A;

Detailed Description Text (10):
How well the parasitics are cancelled depends to a large degree on how accurately the relationship C.sub.C =1/6 C.sub.P is realized. This requires an accurate estimation of the value of C.sub.P and an accurate lay out of capacitor C.sub.C. The present invention provides a novel method of implementing the compensation capacitor C.sub.C to maximize the accuracy in cancelling the parasitic capacitance due to the polysilicon resistors in the RMC integrator. Referring to FIG. 6, there is shown a schematic representation of how compensation capacitor C.sub.C is implemented according to the present invention. A polysilicon dummy resistor R.sub.D with a value equal to one sixth of the value of the main resistor to be compensated is utilized to replicate the parasitic conditions of the main resistor. Dummy resistor R.sub.D is formed of polysilicon layer 604 and is laid on top of a dielectric layer 602 such as silicon dioxide. Polysilicon layer 604 is drawn using the identical

finger size (length l, width w) as the main resistor. Dummy resistor R.sub.D is drawn in a dedicated well, shown in the exemplary embodiment of FIG. 6 as n-type well 600 inside a p-type substrate 610. The separate n-wells for the main and the dummy resistors minimize any noise coupling from the substrate. The two ends of the dummy resistor are electrically shorted together and form one electrode 606 of the compensation capacitor C.sub.C, while an n.sup.+ contact 608 to n-well 600 forms the other electrode of the compensation capacitor.

Detailed Description Text (13):
In another embodiment, the present invention provides an improved tuner circuit for tuning out any variations in the time constant of the RMC integrator caused by variations in any of its components. The tuner circuit of the present invention is based on a phase-locked loop (PLL) design and is fully differential to supply differential control signals to the RMC integrator. FIG. 7A shows the tuner circuit according to one embodiment of the present invention which provides several significant improvements over the tuner circuit of FIG. 1.

Detailed Description Text (14):
The tuner circuit according to the embodiment of the present invention shown in FIG. 7A includes a low-impedance differential charge-pump 122 instead of the high-impedance single-ended charge-pump of the conventional tuner circuit (106 in FIG. 2). Differential charge pump 122 includes a differential opamp 124 whose differential outputs supply the differential control signals V.sub.CP and V.sub.CM. A differential current source circuit connects to the inputs of differential opamp 124. A first pair of switched current sources 126 and 128 couple to one input of opamp 124, and a second pair of switched current sources 130 and 132 connect to the other input of opamp 124. The outputs of phase detector 104, Up and DN, control the state of current source switches. In addition to the common-mode feedback circuit that is internal to differential opamp 124, the differential current source section includes a separate common-mode feedback that is implemented using the block CMF 125 as shown.

Detailed Description Text (15):
In operation, charge pump circuit 122 receives the control signals UP and DN which switch the differential current. After being integrated on the feedback capacitors C, the signal generates positive or negative change in the differential control voltage V.sub.CP -V.sub.CM. With this implementation, even if some mismatch exists between sinking current source (126) and sourcing current sources (128), the output common-mode voltage of the charge pump circuit is independently determined by the opamp, while the differential voltage V.sub.CP -V.sub.CM is controlled by the difference between the sinking and sourcing current sources. The charge pump circuit as thus implemented generates a voltage as opposed to current output signal and exhibits low-impedance at its output. Thus, the control voltages V.sub.CP and V.sub.CM are much less susceptible to noise.

Detailed Description Text (17):
An exemplary implementation for the differential current source structure of charge pump 122 is shown in FIG. 7B. The circuit is made up of a differential folded cascode circuit that receives control signals UP and DN at gate terminals of a differential pair of MOS transistors M2 and M3, respectively. Cascode transistors M61/M62 implement switched current source 126, transistors M71/M72 implement switched current source 130, transistors M41/M42 implement current source 128, and transistors M51/M52 implement switched current source 132. The outputs OUTP and OUTM connect to the positive and negative inputs of opamp 124 and CMF block 125. The common mode feedback signal CMFIN is applied to gate terminals of transistors M61 and M71 as shown. For purposes of this description, assuming that the current in current source devices M11, M41 and M51 are equal and twice as that of current source devices M61 and M71. When signal UP is logic high and DN is logic low, transistor M2 turns OFF while M3 is ON. As a result, the full current of M11 flows through M41 turning M42 OFF. Consequently, the sourcing current of current source transistor M61 flows out through its cascode device M62 and through OUTP terminal while the sinking current of transistor M51 flows in through its cascode device M52 and OUTM output terminal. For the case where UP input is logic low and DN input is logic high, the current of current source devices M11 fully flows through device M51 turning cascode transistor M52 OFF. As a result the current at output terminal OUTP

flows in through cascode transistor M42 and sinking current source transistor M41, while that of terminal OUTM flows out through sourcing current source M71 and its corresponding cascode device M72. This current sourcing and sinking action is integrated on feedback capacitors of opamp 124 (FIG. 7A) generating control voltages V.sub.CP and V.sub.CM for tuning circuit 136. For the case where UP and DN inputs are both logic high no current is flowing in or out of terminals OUTP and OUTM.

Detailed Description Text (22):
In conclusion, the present invention provides various circuit techniques to implement continuous-time filters with improved performance. According to the invention, RMC integrators use wide bandwidth high-gain differential opamps and accurate compensation capacitors to minimize bandwidth limiting factors and to achieve lower harmonic distortion. An on-chip tuner with a differential charge pump circuit provides a low-impedance control-voltage. While the above provides a complete description of several specific embodiments of the present invention, it is possible to use various alternatives, modifications and equivalents. Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents.

Other Reference Publication (3):
"Monolithic Phase-Locked Loops and Clock Recovery Circuits," edited by Behzad Razavi, IEEE Press, 1996, p. 1 and pp. 28-29.

CLAIMS:

1. A differential tuner circuit comprising:

a differential voltage-controlled oscillator (VCO) having first and second control input terminals and first and second output terminals;

a comparator having first and second input terminals respectively coupled to said first and second output terminals of said differential VCO, and an output terminal;

a phase detector having a first input terminal coupled to said output terminal of said comparator, a second input terminal coupled to receive an external signal, and first and second output terminals; and

a differential charge pump circuit having first and second control input terminals respectively coupled to said first and second output terminals of said phase detector, and a differential output having a first output terminal supplying a voltage signal Vcp and a second output terminal supplying a voltage signal Vcm, said differential output being coupled to said first and second control input terminals of said differential VCO,

wherein said differential charge pump circuit comprises:

a fully differential operational amplifier having first and second input terminals, and first and second output terminals respectively coupled to supply voltage signals Vcm and Vcp;

a first pair of switched current source devices coupled to said first input terminal of said fully differential operational amplifier; and

a second pair of switched current source devices coupled to said second input terminal of said fully differential operational amplifiers,

wherein, said differential VCO operates in response to differential signal Vcp-Vcm.

2. The differential tuner circuit of claim 1 wherein said differential charge pump circuit further comprises:

a common-mode feedback circuit coupled between said first and second input terminals and said first and second pair of switched current source devices;

a first RC feedback network coupled between said first input terminal and said first output terminal of said fully differential operational amplifier; and

a second RC feedback network coupled between said second input terminal and said second output terminal of said fully differential operational amplifier.

4. The differential tuner circuit of claim 1 wherein said first pair of switched current source devices comprises a first pair of cascode MOS transistors coupled in series with a second pair of cascode MOS transistors, and

wherein, said second pair of switched current source devices comprises a third pair of cascode MOS transistors coupled in series with a fourth pair of cascode MOS transistors.

5. The differential tuner circuit of claim 4 wherein said differential charge pump circuit further comprises a differential pair of input MOS transistors having gate terminals respectively coupled to said first and second output terminals of said phase detector, and drain terminals respectively coupled to said first pair of cascode MOS transistors and said third pair of cascode MOS transistors.

8. A differential tuner circuit comprising:

a differential voltage controlled oscillator coupled to a phase detector; and

a differential charge pump circuit coupled to said phase detector and said differential voltage controlled oscillator, said differential charge pump circuit including a differential current source circuit coupled to a fully differential operational amplifier, said fully differential operational amplifier having a differential output with a first output terminal coupled to supply voltage signal Vcm and a second output terminal coupled to supply voltage signal Vcp, and

wherein said differential charge pump generates a differential control signal Vcp-Vcm in response to signals supplied by said phase detector, and

wherein, said differential voltage controlled oscillator comprises:

a first differential integrator having a pair of differential input terminals, a pair of differential output terminals, and a pair of differential control input terminals respectively coupled to receive said differential control signal Vcp-Vcm;

a second differential integrator having a pair of differential output terminals respectively coupled to said pair of differential input terminals of said first differential integrator, a pair of differential input terminals cross-coupled to said pair of differential output terminals of said first differential integrator, and a pair of differential control input terminals respectively coupled to receive said differential control signal Vcp-Vcm.

9. A differential tuner circuit comprising:

a voltage controlled oscillator coupled to a phase detector; and

a differential charge pump circuit coupled to receive control signals from said phase detector, and coupled to supply a differential control voltage signal to said voltage controlled oscillator, said differential charge pump circuit comprising:

a fully differential operational amplifier having first and second input terminals and first and second output terminals, said first and second output terminals coupled to supply said differential control voltage signal,

a differential current source circuit coupled to said fully differential operational amplifier, said differential current source circuit including:

a differential input stage having a pair of source-coupled MOS input transistors with gate terminals respectively coupled to receive said control signals from said phase detector,

a first pair of cascode-coupled current source MOS transistors having a common node coupled to a first output terminal of said differential input stage,

a second pair of cascode-coupled current source MOS transistors having a common node coupled to a second output terminal of said differential input stage,

a third pair of cascode-coupled MOS transistors coupled in series with said first pair of cascode-coupled current source MOS transistors, and

a fourth pair of cascode-coupled MOS transistors coupled in series with said second pair of cascode-coupled current source MOS transistors, and

a common-mode feedback circuit coupled between said first and second input terminals of said fully differential operational amplifier and said third and fourth pair of cascode-coupled MOS t transistors.

L7: Entry 7 of 38 File: USPT Oct 20, 1998

DOCUMENT-IDENTIFIER: US 5825640 A
TITLE: Charge pump circuit and method

Abstract Text (1):
A circuit and method produce a pump current (I.sub.p) at the output (31) of a charge pump (26). A switching transistor (32, 35) is coupled at a node (38, 39) to a current source transistor (33, 34) to produce the pump current at a specified magnitude in response to an input pulse (V.sub.PU, V.sub.PD). A charge is stored on a parasitic capacitance of the node. A charge conduction path (42, 43) is coupled to the node and enabled on one transition edge of the input pulse to alter the charge by routing to a discharge node (45) to reduce charge flowing to the output as an error current. The charge conduction path is disabled on the other transition edge of the input pulse to isolate the node from the output.

Application Filing Year (1):
1997

Brief Summary Text (2):
The present invention relates in general to integrated circuits, and more particularly to a circuit for reducing error in a charge pump circuit.

Brief Summary Text (3):
Portable wireless communications systems are using digital techniques to increase system functionality while reducing manufacturing cost. For example, pagers can reduce the number of external tuning components by using digital tuning to select a radio frequency (RF) carrier signal modulated with an audio or video signal. A phase locked loop or frequency synthesizer includes a voltage controlled oscillator (VCO) for producing a local oscillator signal which is mixed with the RF signal to produce an intermediate frequency (IF) signal from which the audio and video signals are extracted. A digital phase/frequency detector compares the phase relationship between the local oscillator signal and a reference signal to produce digital detection pulses which are converted to proportional pump current pulses at the output of a charge pump. A loop filter develops the pump current pulses into an analog control voltage for adjusting the VCO to align the frequencies of the local oscillator and reference signals.

Brief Summary Text (4):
The pump current is kept at a low magnitude to minimize current drain and to allow fine adjustments to be made to the VCO for reducing phase noise when the local oscillator and referenced signals are locked. However, such low current operation increases the sensitivity to pump current errors arising when charge stored on parasitic capacitances in the charge pump flows to the output in response to an input switching transition. For example, at the trailing edge of a detection pulse, parasitic capacitance delays the current switch from turning off until the stored charge is depleted by flowing through the current switch to the output as an error current. The error current is integrated and applied to the VCO, increasing phase jitter in the local oscillator signal and producing demodulation errors in the communications device.

Brief Summary Text (5):
Prior art charge pumps reduce such error currents by routing the stored charge away from the charge pump output through a discharge capacitor after a detection pulse transition. A problem with prior art charge pumps is that the discharge capacitor adds even more parasitic capacitance to the current switch, which increases the amount of stored charge. Even though the discharge capacitor reduces error at the

trailing edge of the detection pulse, the increased charge across the capacitor flows to the output as a pump current error at the leading edge of the detection pulse.

Brief Summary Text (6):
Hence, there is a need for an improved charge pump operating at a low current level and having a reduced pump current error to reduce system noise in a portable communications device.

Drawing Description Text (4):
FIG. 3 is a schematic diagram of a charge pump circuit;

Drawing Description Text (5):
FIG. 4 is a timing diagram of charge pump signals;

Drawing Description Text (7):
FIG. 6 is a schematic diagram of another charge pump; and

Drawing Description Text (8):
FIG. 7 is a schematic diagram of yet another charge pump.

Detailed Description Text (3):
FIG. 2 is a block diagram of local oscillator 110 configured as a phase locked loop and including a voltage controlled oscillator (VCO) 22, a phase/frequency detector (PFD) 24, a charge pump 26 and a filter circuit 28 for implementing on an integrated circuit. In the figures, elements having the same reference number perform similar functions. Local oscillator signal V.sub.LO is generated at the output of VCO 22 for applying to an input of PFD 24. The V.sub.LO frequency is adjusted by integrating a pump current I.sub.p with filter 28 to derive an analog control signal V.sub.CONTROL applied to a control input of VCO 22.

Detailed Description Text (7):
Charge pump 26 operates as a current switch that switches current pulses of a predetermined amplitude to produce pump current I.sub.p in response to detection pulses UP and DOWN. An I.sub.p current pulse has the same pulse width as a pulse of UP or DOWN, and therefore is also proportional to the phase difference between V.sub.LO and V.sub.REF. The I.sub.p pulses effectively supply charge packets of one polarity in response to UP and the opposite polarity in response to DOWN. The charge packets are integrated by filter 28 to produce V.sub.CONTROL. For example, when UP is active, I.sub.p may supply a current that increases the charge on filter 28, so that when DOWN is active, I.sub.p has the opposite polarity to reduce the charge on filter 28.

Detailed Description Text (8):
Filter 28 is shown as comprising an impedance circuit 27 and a capacitor 29 serially coupled between the output of charge pump 26 and ground. Capacitor 29 provides the integrating function, storing the charge packets from charge pump 26. Impedance circuit 27 includes components which provide a desired loop response and which increase the phase margin to ensure loop stability. It should be evident that filter 28 could alternatively be implemented using active components such as amplifiers or using a more complex network of passive components, depending on system requirements. The I.sub.p charge packets are proportional to the phase difference between V.sub.LO and V.sub.REF to reduce the lock time of local oscillator 110 by providing a greater adjustment in V.sub.CONTROL when V.sub.LO and V.sub.REF are farther apart in phase or frequency.

Detailed Description Text (9):
I.sub.p is set to a low current level to make finer adjustments to V.sub.CONTROL when V.sub.LO and V.sub.REF are locked, thereby reducing noise and extending the time between battery recharges. Such low current operation increases the sensitivity to pump current errors arising when charge stored on parasitic capacitances flows to the output of the charge pump. The parasitic capacitances include junction and gate oxide capacitance as well as accumulation charge stored in the channels of transistors of the charge pump. Such charges are pump current errors because the resulting pump current pulse is not proportional to the phase difference between the

local oscillator and reference frequencies. The pump current errors are developed by the filter into a corresponding error in the VCO control voltage which causes an overadjustment of the VCO and increases phase jitter and noise.

Detailed Description Text (10):
For example, a typical prior art charge pump includes a current conduction path for supplying the pump current to the output of the charge pump. The current conduction path includes a switching transistor responsive to a detection pulse and coupled at a switching node to a current source transistor biased to set the pump current level. At the leading edge of a detection pulse, the switching transistor is enabled to provide a relatively low impedance to rapidly charge the parasitic capacitance, thereby producing a minimal pump current error. However, at the trailing edge, the switching transistor is disabled, which sets the switching node to a high impedance state. The stored charge flows to the output through the current source transistor, which momentarily continues to conduct until the charge is depleted. A filter integrates the error to produce a corresponding error in the VCO control voltage, causing an overadjustment of the VCO and increasing phase jitter and noise.

Detailed Description Text (11):
One prior art charge pump reduces the error by routing the stored charge through a capacitor coupled to the switching node. The capacitor often is implemented with a transistor structure having a common drain-source connection operating as one capacitor electrode and a gate operating as the other capacitor electrode. However, such a capacitor adds substantial capacitance to the switching node, which results in more charge being stored. Because the capacitor is enabled on both transitions of the detection signal, the increased charge on the switching node delays turning on the switching transistor to produce a pump current error at the leading edge of the detection pulse.

Detailed Description Text (12):
FIG. 3 is a schematic diagram of charge pump 26 providing I.sub.p current pulses at an output 31, and including transistors 32-37. V.sub.PBIAS and V.sub.NBIAS are generated in a regulator circuit (not shown) to set the amplitude of the I.sub.p pulses. In one embodiment, I.sub.p has a value of ten microamperes set by a transistor gate-source voltage of 0.8 volts, such that transistor 33 is biased at V.sub.PBIAS =V.sub.DD -0.8=2.2 volts to supply ten microamperes of charging current. V.sub.NBIAS is set to 0.8 volts so that transistor 34 supplies ten microamperes of discharging current when enabled. Therefore, I.sub.p can have a value of zero or plus or minus ten microamperes. Switching signals V.sub.PU and V.sub.PD are derived from, and have similar pulse widths, as UP and DOWN, as described below. V.sub.PU is active when at a logic low level and V.sub.PD is active at a logic high level.

Detailed Description Text (13):
Those skilled in the art understand that transistors have a conduction path formed between first and second conduction electrodes which is modified with a control voltage applied to a control electrode of the transistor. For example, in a metal-oxide-semiconductor transistor, the first and second conduction electrodes correspond to the drain and source electrodes of the transistor and the control electrode corresponds to the gate electrode. A channel formed between the drain and source provides the conduction path, which is activated or enabled when a voltage greater than a conduction threshold of the transistor is applied across the gate and source electrodes. The conduction path is deactivated or disabled when a voltage less than the conduction threshold is applied.

Detailed Description Text (14):
The operation of charge pump 26 is seen by referring to the timing diagram of FIG. 4. Transistors 32 and 35 operate as switches in response to V.sub.PU and V.sub.PD, respectively, to enable I.sub.p current pulses through transistors 33 and 34 to output 31. Transistors 32 and 35 have nearly zero volts from drain to source when switched on. Initially, at time T.sub.0, V.sub.PU and V.sub.PD are inactive and I.sub.p is zero. At time T.sub.1, V.sub.PU is activated to turn on transistor 32 and produce an I.sub.p pulse, shown in FIG. 4 as having a positive magnitude. At time T.sub.2, V.sub.PU terminates and transistors 32 and 33 are switched off, restoring I.sub.p to zero current. Similarly, at time T.sub.4, V.sub.PD is active, switching on transistors 35 and 34 to produce I.sub.p having a negative magnitude as shown. At

time T.sub.5, V.sub.PD terminates and transistors 35 and 34 are switched off, again restoring I.sub.p to zero current. As shown in FIG. 3, node 38 is a switching node whose parasitic capacitance is charged through switching transistor 32, which is enabled at the leading edge of V.sub.PU to provide a low impedance charging path. Similarly, node 39 is a switching node whose parasitic capacitance is charged through transistor 35, which is enabled at the leading edge of V.sub.PD to provide a low impedance path.

Detailed Description Text (15):
The present invention improves on prior art charge pumps by routing the stored charge through a charge conduction path to a discharge node on the trailing edge of the detection pulse, while disabling the charge conduction path to isolate the switching node from the discharge node at the leading edge. For example, transistor 37 operates as a charge conduction path which alters the stored charge on node 38 by routing the charge through transistor 37 to a discharge node, i.e., ground, in response to V.sub.PPULSE. Similarly, transistor 36 operates as a charge conduction path to alter the stored charge on node 39 by routing the charge through transistor 36 to a discharge node, i.e., V.sub.DD, in response to V.sub.NPULSE. Transistors 37 and 36 typically are small transistors which add minimal capacitance to nodes 38 and 39 in comparison to the capacitor circuits of prior art charge pumps.

Detailed Description Text (16):
The leading edge of V.sub.PPULSE coincides with the trailing edge of V.sub.PU. V.sub.PPULSE terminates before the next detection pulse, so transistor 37 is disabled before V.sub.PU again becomes active, thereby isolating node 38 from ground to prevent a delay in enabling transistor 33. The leading edge of V.sub.NPULSE commences at the trailing edge of V.sub.PD. V.sub.NPULSE terminates before the next detection pulse, so transistor 36 is disabled while V.sub.PD is active, which isolates node 39 from V.sub.DD to prevent a delay in enabling transistor 34. V.sub.PPULSE is derived from UP as described below to terminate after a few gate delays to allow charge pump 26 to stabilize before the next detection pulse and to prevent transistors 32 and 37 from being enabled at the same time to generate an undesirable current spike. Similarly, V.sub.NPULSE is derived from DOWN to terminate after a few gate delays to allow charge pump 26 to stabilize before the next cycle and to prevent transistors 35 and 36 from being enabled at the same time.

Detailed Description Text (21):
The discharging of switching nodes to either V.sub.DD or ground potential reduces the output dynamic range of the charge pump. In particular, as the output approaches ground potential, the current source transistor becomes forward biased to form a channel that causes the transistor to operate in the inverse mode. The channel couples the output to the switching node, which drains charge from the output to equalize the potentials of the output and the switching node. The amount of drained charge is determined by the voltage across the channel. In particular, the drained charge increases as the difference between the switching node and output potentials increases. Because the switching node is discharged to the same potential as the discharge node, the drained charge increases as the difference between the switching and discharge nodes increases. For example, assume that a switching node is discharged to V.sub.DD, so that when the output approaches ground, a total of V.sub.DD -0.0=3.0 volts is applied across the channel of the inverted device. If another switching node is discharged to ground and the output approaches V.sub.DD, a total of V.sub.DD -0.0=3.0 volts is applied across the channel of the inverted current source device.

Detailed Description Text (22):
FIG. 6 is a schematic diagram of charge pump 26 in an alternate embodiment having an increased dynamic range, including transistors 32-35 and 40-41. Transistors 32-35 operate as described in the embodiment of FIG. 3. Pulse signals V.sub.PPULSEB and V.sub.NPULSEB are inverted forms of V.sub.PPULSE and V.sub.NPULSE which are generated by a circuit similar to pulse generator circuit 50. Hence, V.sub.PPULSEB and V.sub.NPULSEB have timing similar to V.sub.PPULSE and V.sub.NPULSE, as shown in FIG. 4. The increased dynamic range results from configuring V.sub.PBIAS =V.sub.DD -0.8=2.2 volts and V.sub.NBIAS =0.8 volts to also operate as discharge nodes as shown.

Detailed Description Text (24):
Charge pump 26 has a further benefit of reduced voltage swings at nodes 38 and 39 which result in faster operation. In particular, node 38 swings from ground to V.sub.NBIAS, or 0.8 volts, and node 38 swings from V.sub.DD =3.0 volts to V.sub.PBIAS =2.2 volts, or 0.8 volts. The smaller swing turns transistors 33 and 34 off more quickly to divert more of the stored charge to the discharge node to further reduce I.sub.p error.

Detailed Description Text (25):
FIG. 7 is a schematic diagram of charge pump 26 in another embodiment, including transistors 32-35 and 42-43 and an amplifier 44. Transistors 32-35 have similar operation as described in FIG. 3. Transistors 42 and 43 are activated by V.sub.PPULSEB and V.sub.NPULSEB to alter the stored charges by discharging nodes 38 and 39. Amplifier 44 is a unity gain amplifier which produces an output voltage at node 45 which operates as a discharge node having a potential substantially equal to that of output 31. The drain electrodes of transistors 42 and 43 are coupled for discharging nodes 38 and 39 to node 45.

Detailed Description Text (26):
As described above, when output 31 approaches V.sub.DD or ground, transistor 33 or 34 is inverted, which produces a conduction path at node 38 or 39 to drain charge from output 31. That is, when output 31 approaches ground, transistor 34 inverts and charge flows between output 31 and node 39 to equalize their potentials. By discharging node 39 to node 45, whose potential equals that of output 31, no charge flows in the channel that is drained from output 31. Similarly, node 38 is discharged to node 45 at the same potential as output 31. Therefore, the charge drained as output 31 approaches V.sub.DD is zero. Because zero error is generated, output 31 can swing closer to V.sub.DD or ground, thereby increasing the dynamic range of charge pump 26.

Detailed Description Text (27):
By now it should be appreciated that the present invention provides an improved charge pump circuit and method for producing a pump current at the output of the charge pump. A current source transistor is coupled at a node to a switching transistor to provide a current conduction path that produces a pump current of a specified magnitude in response to an input pulse. A charge is stored on parasitic capacitance of the node. A discharge transistor reduces pump current error by providing a charge conduction path which is enabled on one transition edge of the input pulse to alter the charge by routing to a discharge node. The charge conduction path is disabled on the other transition edge to isolate the node from the output.

Other Reference Publication (2):
Floyd M. Gardner, "Charge-Pump Phase-Lock Loops", IEEE Transactions on Communications, vol. COM-28, No. 11, Nov. 1980, pp. 321-330.

CLAIMS:

1. A charge pump, comprising:

a first current conduction path responsive to a first input pulse for supplying a pump current to an output of the charge pump; and

a charge circuit coupled to a first node of the first current conduction path where the charge circuit is disabled during a first transition of the first input pulse and enabled during a second transition of the first input pulse to alter a charge on the first node.

2. The charge pump of claim 1, wherein the charge circuit includes a first transistor having a control electrode responsive to the first input pulse and a conduction path coupled to the first node for routing the charge to a first discharge node of the charge pump.

3. The charge pump of claim 2, further comprising an amplifier having an input coupled to the output of the charge pump and an output for setting a potential of

the first discharge node equal to a potential of the output of the charge pump.

4. The charge pump of claim 2, wherein the first current conduction path further comprises:

a first current source transistor having a control electrode coupled for receiving a first bias voltage, a first conduction electrode coupled to the first node, and a second conduction electrode for providing the pump current; and

a first switching transistor having a control electrode responsive to the first input pulse for modifying a conduction path coupled between the first node and the first discharge node.

5. The charge pump of claim 4, wherein the first input pulse is received at an input of the first current conduction path, further comprising a pulse generator including:

a delay line having an input responsive to the first input pulse and an output for producing a delayed pulse after a specified delay; and

a first logic gate having a first input coupled for receiving the first input pulse, a second input coupled for receiving the delayed pulse, and an output coupled to the input of the first current conduction path for producing a discharge pulse that terminates after the specified delay.

6. The charge pump of claim 4, further comprising:

a second current source transistor having a control electrode coupled for receiving a second bias voltage, a first conduction electrode coupled to a second node, and a second conduction electrode coupled to the output of the charge pump; and

a second switching transistor having a control electrode responsive to a second input pulse for modifying a conduction path coupled between the second node and a power supply conductor.

7. The charge pump of claim 6, wherein the charge circuit further comprises a second transistor having a control electrode responsive to the second input pulse and a conduction path coupled between the second node and a second discharge node.

8. The charge pump of claim 1 where the charge pump is disposed on an integrated circuit.

9. The charge pump of claim 8 where the integrated circuit includes:

a phase detector for sensing a phase between an oscillator signal and a reference signal to produce the first and second input pulses ; and

a voltage controlled oscillator (VCO) operating in response to the pump current for providing the oscillator signal at an output.

10. An integrated circuit including a charge pump, the charge pump comprising:

a first current conduction path responsive to a first input pulse for supplying a first pump current to an output of the charge pump;

a first pulse generator having an input coupled for receiving the first input pulse and an output providing a first control signal that is inactive during a first transition of the first input pulse and active during a second transition of the first input pulse; and

a first charge conduction path coupled to a node of the first current conduction path to alter a charge on the node and having a control input coupled for receiving the first control signal from the pulse generator.

11. The integrated circuit of claim 10, further comprising:

a phase detector having first and second inputs respectively coupled for receiving an oscillator signal and a reference signal, and a first output for providing the first input pulse when the oscillator signal leads the reference signal in phase; and

a voltage controlled oscillator having a control input coupled to the output of the charge pump for providing the oscillator signal at an output.

12. The integrated circuit of claim 11, wherein the phase detector has a second output for providing a second input pulse when the oscillator signal lags the reference signal in phase, further comprising:

a second current conduction path responsive to the second input pulse for supplying a second pump current to the output of the charge pump;

a second pulse generator having an input coupled for receiving the second input pulse and an output providing a second control signal that is inactive during a first transition of the second input pulse and active during a second transition of the second input pulse; and

a second charge conduction path coupled to a node of the second current conduction path to alter a charge on the node and having a control input responsive to the second control signal.

14. The integrated circuit of claim 13, wherein the first and second charge conduction paths route the charges on the first and second nodes, respectively, to a discharge node, further comprising an amplifier having an input coupled to the output of the charge pump and an output for setting a potential of the discharge node equal to a potential of the output of the charge pump.

15. A wireless communication device, comprising

a receiver circuit having a first input coupled for receiving a radio frequency (RF) signal modulated with information, a second input coupled for receiving a local oscillator signal for mixing with the RF signal to produce an intermediate frequency (IF) signal, and including a demodulator for extracting the information from the IF signal;

a voltage controlled oscillator having an output for providing the local oscillator signal at a frequency determined by a control signal;

a phase detector operating in response to the local oscillator signal and a reference signal, and having a first output for providing a first detection pulse when the local oscillator signal leads the reference signal in phase;

a charge pump, including:

(1) a first current conduction path responsive to the first detection pulse for supplying a first pump current to an output of the charge pump; and

(2) a first charge circuit coupled to a first node of the first current conduction path where the first charge circuit is disabled during a first transition of the first detection pulse and enabled during a second transition of the first detection pulse to alter a charge on the first node.

16. The wireless communications device of claim 15, wherein the first detection pulse is received at an input of the current conduction path, and the charge pump further comprises a pulse generator including:

a delay line having an input responsive to the first detection pulse and an output for producing a delayed pulse after a specified delay; and

a first logic gate having a first input coupled for receiving the first detection pulse, a second input coupled for receiving the delayed pulse, and an output coupled

to the input of the first current conduction path for producing a discharge pulse that terminates after the specified delay.

17. The wireless communications device of claim 16, wherein the phase detector has a second output for providing a second detection pulse when the oscillator signal lags the reference signal in phase, the charge pump further comprising:

a second current conduction path responsive to the second detection pulse for supplying a second pump current to the output of the charge pump such that the first and second pump currents have opposite polarities;

a second pulse generator having an input coupled for receiving the second detection pulse and an output providing a second control signal that is inactive during a first transition of the second detection pulse and active during a second transition of the second detection pulse; and

a second charge conduction path coupled to a node of the second current conduction path to alter a charge on the node and having a control input responsive to the second control signal.

18. A method of generating a charge pump current through a current conduction path in response to an input pulse, comprising the steps of:

disabling a charge conduction path from a node of the current conduction path during a first transition of the input pulse; and

enabling the charge conduction path during a second transition of the input pulse to alter a charge on the node.

23. The method of claim 22, wherein the step of developing includes a step of filtering the charge pump current.

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- US Patents Full-Text Database
- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Term:
```
(state near2 frequenc$3 near3 control$3 near4 (pll
or (phase adj lock$3 adj loop$)))
```

Display: 62 **Documents in Display Format:** - **Starting with Number** 1

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Search History

DATE: Friday, May 02, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L17	(state near2 frequenc$3 near3 control$3 near4 (pll or (phase adj lock$3 adj loop$)))	17	L17
L16	L15 and l11	92	L16
L15	(state near3 control$3 near4 (pll or (phase adj lock$3 adj loop$)))	217	L15
L14	(battery) near3 (control$3 near pll)	1	L14
L13	((broadband or broad adj band) same (pll or (phase near2 lock$3 near2 loop$))) and (phase near2 differenc$3) and (frequenc$3 near2 difference$)	36	L13
L12	L11 and l10	90	L12
L11	(375/$3.ccls. or 331/$4.ccls. or 327/$4.ccls.)	132078	L11
L10	((broadband or broad adj band) and (pll or (phase near2 lock$3 near2 loop$))) and (phase near2 differenc$3) and (frequenc$3 near2 difference$)	205	L10
L9	((broadband or broad adj band) same (pll or (phase near2 lock$3 near2 loop$))) same (phase near2 differenc$3) same (frequenc$3 near2 difference$)	0	L9
L8	((broadband or broad adj band) near4 (pll or (phase near2 lock$3 near2 loop$))) same (phase near2 differenc$3) same (frequenc$3 near2 difference$)	0	L8
L7	(phase near lock$3 near loop$3) and (frequenc$3 near lock$3 near loop$3) and (charge near2 pump$3) and (power near2 suppl$3)	39	L7
L6	(phase near2 lock$3 near2 loop$3) and (frequenc$3 near2 lock$3 near2 loop$3) and (charge near2 pump$3) and (power near2 suppl$3)	142	L6
L5	(phase near2 lock$3 near2 loop$3) same (frequenc$3 near2 lock$3 near2 loop$3) same (charge near2 pump$3) same (power near2 suppl$3)	2	L5
L4	(phase near2 lock$3 near2 loop$3) same (frequenc$3 near2 lock$3 near loop$3) same (charge near2 pump$3) same (power near2 suppl$3)	2	L4
L3	(phase near2 lock$3 near2 loop$3) same (frequenc$3 near2 lock$3 near loop$3) same (voltage near3 convert$3) same (current near3 convert$3) same (charge near2 pump$3) same (power near2 suppl$3)	0	L3
L2	(phase near2 lock$3 near2 loop$3) same (frequenc$3 near2 lock$3 loop$3) same (voltage near3 convert$3) same (current near3 convert$3) same (charge near2 pump$3) same (power near2 suppl$3)	2	L2
L1	(phase near2 lock$3 near2 loop$3) same (frequenc$3 near2 lock$3 loop$3) same (voltage near3 convert$3) same (current near3 convert$3) same (charge near2 pump$3)	75	L1

END OF SEARCH HISTORY